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Streamlined Advanced Semiconductor FA Through In-Situ CAFM and Plasma FIB Integration

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Abstract

This work presents a streamlined and efficient failure analysis methodology for advanced integrated circuits by integrating an in-situ CAFM-pFIB platform. This approach eliminates repeated vacuum cycles and manual transfers, significantly reducing analysis time while preserving pristine surfaces for high-quality CAFM imaging. The system's effectiveness was validated through case studies, including one on a stacked-die package where pFIB milling was used not only for in-situ delayering across multiple layers but also for creating a grounding path to enable successful CAFM localization of leaky gate defects. This integrated platform also made possible a novel Scanning EBIC Microscopy technique for mapping subsurface junction behavior, offering new capabilities for nanoscale defect localization in complex semiconductor technologies.

Introduction

The continued scaling of transistor dimensions in advanced semiconductor technologies introduces significant challenges in failure analysis (FA). As device geometries shrink and feature densities increase, the defects become increasingly subtle, making conventional FA method less effective. Furthermore, the growing complexity of modern integrated circuits, driven by innovations in chip design and device architecture, has given rise to more intricate failure mechanisms. To meet the demands of rapid yield ramp and continuous reliability enhancement, novel FA techniques must be explored and developed.

Among traditional methods, electron-beam and ion-beam based passive voltage contrast (PVC) techniques have been employed for defect localization [1]. However, their efficacy diminishes significantly at advanced technology nodes due to their limited sensitivity to reliably detect electrically subtle or buried defects.

In this context, conductive atomic force microscopy (CAFM) has emerged as a useful technique for addressing the limitations of conventional PVC approaches. CAFM offers both high spatial resolution and electrical sensitivity, making it particularly helpful for analyzing defects in FinFETs and other nanoscale devices. The operational principle of CAFM is illustrated schematically in Figure 1. A sharp conductive probe is raster-scanned across the sample surface while a bias voltage is applied between the probe and the sample. At each scan point, the probe measures the local electrical current, allowing a construction of current mapping in parallel with the topographical map [2].

Figure 1 also presents example topography and current images acquired from an integrated circuit (IC) sample. Notably, a single current image can contain quantitative current data from hundreds or thousands of nanoscale devices, enabling simultaneous electrical characterization and defect localization. This capability significantly enhances the efficiency of semiconductor FA [3-5].

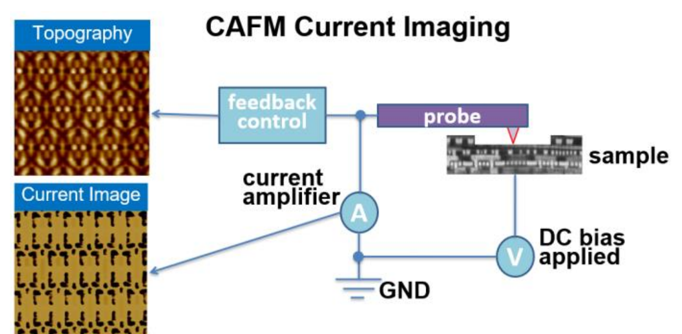

Figure 1. Schematics of CAFM current imaging

A compelling demonstration of CAFM's effectiveness is presented in Figure 2. Initially, SEM-based passive voltage contrast (PVC) imaging was employed; however, it failed to detect the defective structure due to its limited sensitivity to subtle electrical anomalies. As illustrated in Figure 2a, the defective via exhibits a contrast nearly identical to that of the reference via-highlighted by the two yellow arrows-thereby masking its presence. In stark contrast, the CAFM current

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images, acquired using a mainstream AFM and depicted in Figure 2b, unambiguously identified the defective via, as indicated by the red arrow. This improved detection is attributable to CAFM's superior sensitivity and its ability to provide quantitative current measurements at each pixel. The quantitative nature of the CAFM data also allows for subsequent extraction of electrical measurement data for further analysis, as exemplified by the current line profile in Figure 2c. In this profile, the defective via is clearly associated with a significantly lower current level compared to the reference via.

This example underscores the substantial advantages of CAFM in both localizing and characterizing electrical defects in advanced semiconductor devices. Its high sensitivity and quantitative capabilities are particularly beneficial at advanced technology nodes where traditional PVC techniques may prove inadequate. While CAFM is a highly effective technique for nanoscale defect localization and electrical characterization, its implementation remains challenging, demanding rigorous sample preparation and precise navigation to the area of interest (AOI).

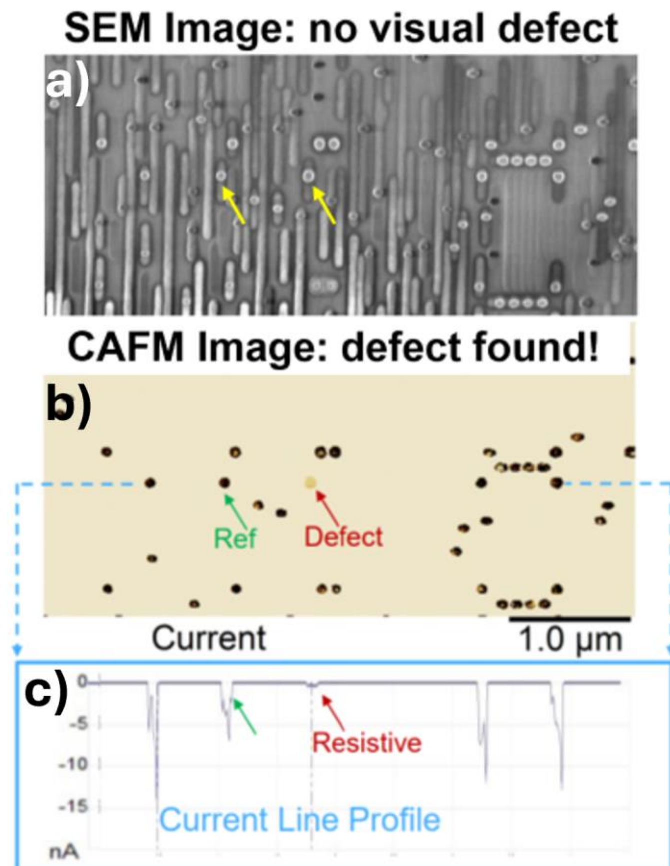

Figure 2. Example showing that CAFM was able to capture a resistive Via defect, while the mainstream SEM PVC technique failed to reveal the same defect

Successful CAFM analysis is contingent upon meticulous sample preparation. The sample must be deprocessed to a level with optimal surface quality to ensure accurate nanoscale electrical contact between the AFM probe tip and the device structures. Because the technique relies on electrical contacts at the nanoscale, the sample surface must be pristine, free from contamination or oxidation. Traditional deprocessing methods based on chemical mechanical planarization (CMP) pose significant challenges in this context. During and after CMP, conductive circuit structures are frequently exposed to ambient conditions, leading to the formation of oxidation layers on exposed metal surfaces. This challenge is further exacerbated by the introduction of new materials at advanced process nodes, such as cobalt contacts, which can easily oxidize upon exposure to the ambient environment [6].

The advent of plasma focused ion beam (pFIB) gas-assisted milling has provided a more precise means of controlling the delayering process. As illustrated in Figure 3, the gas injection system delivers reactive gas through a nozzle to the chamber, enabling the plasma focused ion beam to selectively mill the target area uniformly. Concurrently, an electron beam can be utilized to monitor the delayering progress in real time, allowing analysts to halt material removal at the optimal point for subsequent CAFM analysis [7,8]. However, even with pFIB-prepared samples, challenges remain. The requirement to transfer samples between the pFIB and CAFM chambers exposes them to ambient conditions, increasing the risk of oxidation. Moreover, the process is inherently time-consuming, involving repeated venting and pumping of vacuum chambers- a drawback that is further amplified when multiple circuit levels must be analyzed.

Navigation further compounds these challenges. CAFM imaging relies on raster scanning the probe tip across the sample surface, a method that is inherently slow and can require several minutes to produce a clear image. Analysts must then compare these images with chip layouts and often perform multiple scans to accurately locate the target area. In contrast, scanning electron microscopy (SEM) can acquire images nearly instantaneously and is frequently integrated with computer aided design (CAD) navigation capabilities in modern SEM or SEM/FIB dual beam systems. CAD navigation allows users to select the target location directly from the layout, with the SEM stage automatically positioning itself at the precise AOI.

To address these limitations, this work explores the integration of a small form factor AFM with a plasma FIB/SEM dual beam system. This approach leverages the advantages of both AFM and SEM/FIB systems while mitigating their respective drawbacks. The integrated system enables pFIB delayering, SEM imaging, and CAFM current imaging performed *in-situ* inside a single vacuum chamber. This integration eliminates the need to transfer samples between different instruments and obviates the necessity for stage repositioning after switching between pFIB milling and CAFM analysis, thereby significantly enhancing workflow efficiency. Furthermore, SEM imaging can be used to rapidly navigate to the AOI via CAD guidance, after which the AFM probe is directed to the target area to acquire high-quality current images. Overall, the integration of AFM into a plasma FIB dual beam system represents a substantial advancement in the failure analysis workflow, particularly for advanced semiconductor devices where traditional techniques may prove inadequate.

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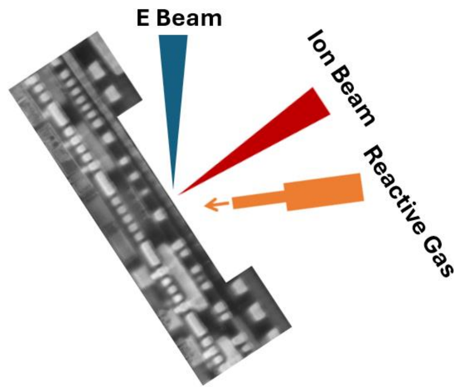

Figure 3. Schematics of pFIB gas assisted delayering for CAFM sample preparation

Experimental

This section details the integrated CAFM-pFIB methodology for streamlined advanced semiconductor failure analysis, involving sequential pFIB delayering and nanoscale CAFM analysis within the same vacuum chamber. This approach aims to enhance efficiency, avoid ambient exposure, and unlock new capabilities, as demonstrated through a targeted analysis on an advanced technology node device using in-situ CAFM imaging of freshly exposed layers following pFIB gas-assisted delayering.

A compact AFM system, equipped with a self-sensing conductive AFM probe tip, was directly mounted onto the stage of a pFIB/SEM dual-beam system. This integrated setup enabled seamless transition between pFIB gas assisted delayering and high-resolution CAFM electrical characterization modes within a single vacuum chamber.

For this experiment, an IC die fabricated using a 5nm-class process technology was extracted from its package. The topmost thick metallization layers were removed using mechanical lapping. Following this initial preparation, the die was mounted onto the AFM stage within the pFIB/SEM system for further deprocessing and analysis.

Precise stage eucentric height alignment at the target area was performed to ensure that the ion beam, electron beam, and AFM probe could all access and scan the same region without interference. Additionally, this alignment allowed for the safe insertion of the gas injection system (GIS) nozzle, which is critical for gas-assisted ion beam milling.

Subsequently, the stage was tilted to 52 degrees-an optimal angle for both Xe plasma FIB milling and SEM imaging. The system was first configured into the milling mode, as illustrated in Figure 4a. In this configuration, the AFM head was retracted and safely parked away from the milling zone, while the GIS nozzle was inserted close to the target area of the sample to deliver the reactive gas needed for enhanced, uniform material removal. Xe plasma ions were then directed to mill a defined area (in this case, a 100 × 100 µm² window) with the presence of the delayering gas.

To precisely control the delayering process, real-time monitoring was conducted using both stage current measurements and ion-beam image-based brightness level within the milled region. SEM imaging was performed intermittently to visually inspect the delayered area and confirm progress, ensuring that the milling process was terminated precisely at the desired circuit level of interest.

Upon completion of the milling process, the system was reconfigured into a switching mode, shown in Figure 4b, in which both the GIS nozzle and the AFM head were returned to their respective parked positions. This intermediate configuration ensured a safe transition between milling and scanning operations.

For CAFM current imaging, the system was switched to the AFM scanning mode, shown in Figure 4c. In this configuration, the GIS nozzle remained in the parked position, while the AFM head was carefully repositioned into the previously delayered target area. With the AFM probe now in place, high-resolution current imaging of the delayered structures could proceed without exposing the sample to ambient conditions or requiring physical repositioning of the sample. This integrated workflow demonstrates the operational efficiency and analytical robustness enabled by embedding a compact AFM module directly into a pFIB/SEM system, particularly for high-resolution failure analysis of advanced semiconductor nodes.

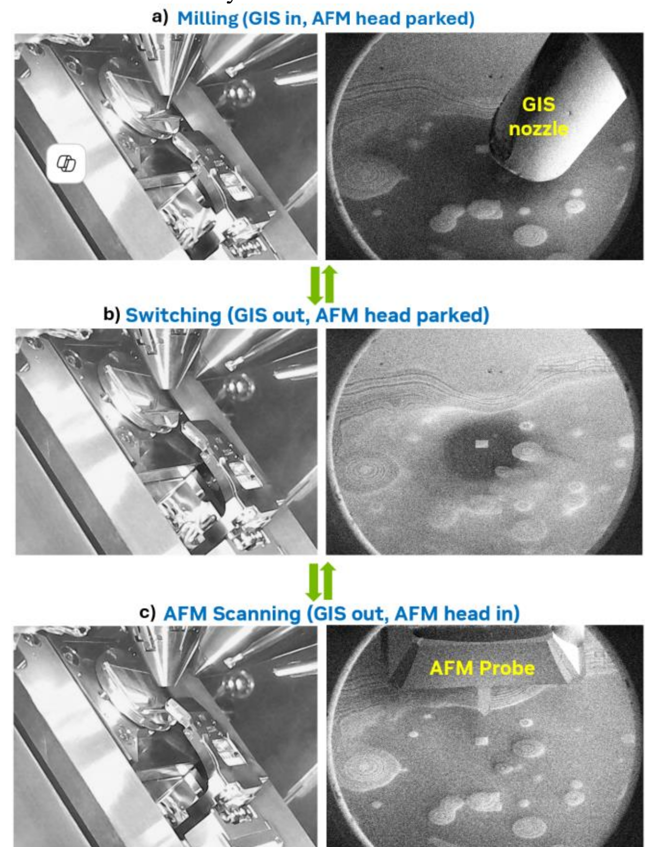

Figure 4. In chamber camera images(left row) and SEM images(right row) for different configurations for a) Milling, b) Switching, and c) AFM Scanning.

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Results and Discussions

Figure 5 presents a sequence of SEM images depicting the target area at three stages: (a) prior to pFIB gas-assisted delayering, (b) after completion of the delayering process, and (c) with the AFM probe positioned for CAFM analysis.

As shown in Figure 5a, the selected region was located at an upper via level within the copper (Cu) metallization stack. To improve efficiency, the thicker top metal layers-often composed of high-density redistribution lines and thick global interconnects-were previously removed by mechanical lapping. This mechanical pre-thinning significantly reduces the time required for subsequent pFIB delayering, as these upper layers would otherwise demand prolonged ion beam milling. Moreover, mechanical lapping offers easier endpoint control at these levels due to the large critical dimensions (CD) of these top layers, making it a practical preprocessing step before pFIB milling.

Following this, Figure 5b shows the same area after gas-assisted pFIB delayering. A 100×100 μm² window was milled to uniformly expose the lower-level circuit structures. The process, which uses Xe plasma ions with tailored reactive gas chemistries, enabled efficient and highly planar material removal. This produced a surface smooth to a scale of tens of nanometers or better, which is desirable for subsequent CAFM analysis.

Figure 5c presents a magnified view of the delayered region with the AFM probe accurately positioned at the milled window, ready for CAFM current imaging. A distinct boundary between the milled and unprocessed regions can be observed. The sidewalls of the delayered window clearly reveal a cross-sectional profile consisting of more than ten metallization layers, providing visual confirmation of the depth and uniformity of the delayering process. Notably, the interior of the milled window exhibits a smooth, uniform, and contamination-free surface, which is ideal for high-resolution CAFM imaging and quantitative current measurements.

Together, these SEM images illustrate the effectiveness of pFIB gas-assisted milling for precise, layer-specific delayering, and highlight the readiness of the sample for integrated AFM-based electrical characterization.

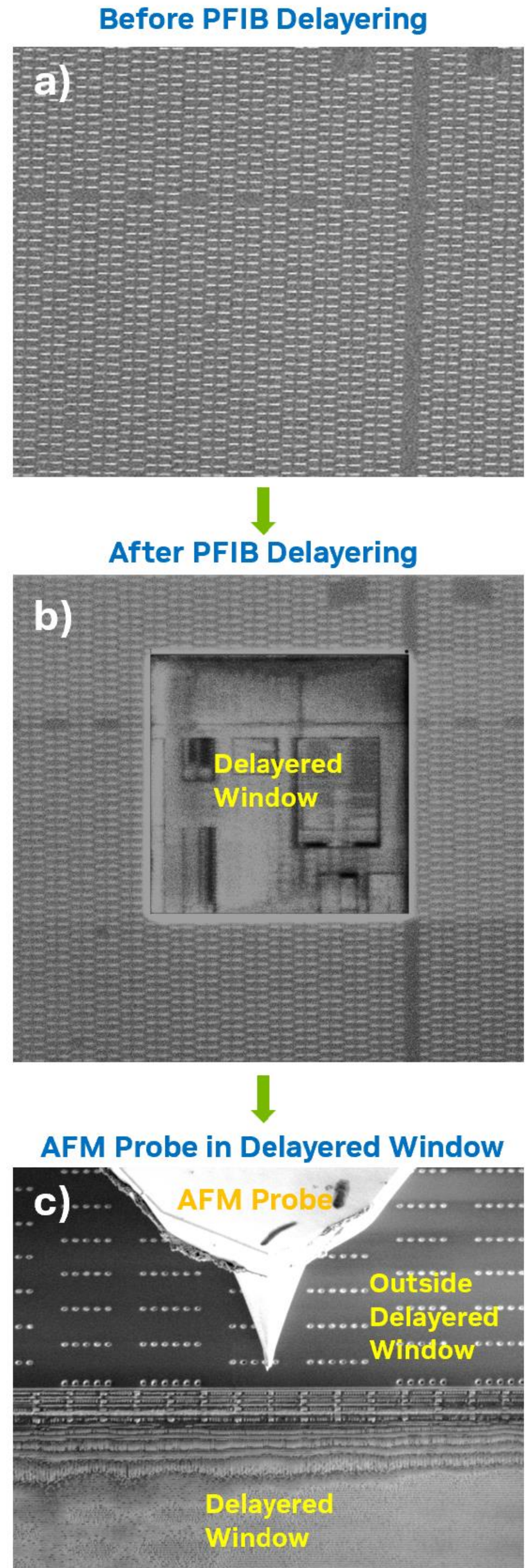

Figure 5. SEM images of the target area a) before pFIB gas assisted delayering, b) after delayering, and c) with AFM probe inserted to the delayered window, ready for AFM analysis.

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In addition to enabling seamless switching between delayering and CAFM analysis, the integration of AFM into a SEM/FIB dual-beam system also significantly enhances the efficiency and accuracy of AFM probe navigation to the AOI. This is particularly valuable for site-specific CAFM analysis targeting an individual transistor, a logic cell, or a memory bit-cell, tasks that are traditionally tedious and time-consuming when performed on a standalone AFM platform.

One of the main challenges in conventional CAFM workflows is the difficulty of navigating the AFM probe to the desired region. AFM imaging relies on raster-scanning the probe across the surface, typically taking several minutes per image. Analysts must then manually compare the acquired AFM topography to the corresponding layout design, often struggling to match features due to the relatively flat and low-contrast surface morphology of delayered samples. This matching process is not only slow but also prone to error, particularly when subtle topographic variations are insufficient to identify unique landmarks.

By contrast, SEM imaging offers a number of advantages that greatly facilitate navigation. SEM images are acquired nearly instantaneously and provide rich structural details, including subsurface information due to material contrast and edge effects. These attributes make it significantly easier to correlate observed features with the layout, thereby streamlining the process of locating specific circuit elements.

Figure 6 illustrates how SEM imaging is leveraged to guide the AFM probe to the exact target location for CAFM analysis. In Figure 6a, following pFIB delayering, the AFM probe is initially positioned near the delayered window. This coarse position can be saved as a reference point, enabling automated return to the same location for subsequent measurements, especially useful in workflows that involve multiple cycles of pFIB delayering and AFM analysis.

In Figure 6b, the probe is gradually moved toward the region of interest under real-time SEM observation. At a 52° stage tilt, standard for SEM/FIB operation, the AFM probe tip is clearly visible in the SEM image, allowing precise tracking and manipulation of its movement. This visual feedback greatly simplifies and accelerates the navigation process compared to conventional standalone AFM systems.

Finally, Figure 6c demonstrates that the AFM probe has been successfully landed on the exact circuit of interest. The SEM-assisted navigation enables accurate targeting without the need for repeated AFM scans, significantly reducing the time and effort required to reach the desired location. Modern FIB/SEM dual beam systems are often equipped with CAD navigation capabilities, enabling synchronization of the sample stage with the CAD layout. This feature can further accelerate the process of navigating the AFM probe to the target area with greater precision and ease.

Once the probe is correctly positioned, CAFM current imaging can be conducted directly at the AOI, allowing for high-resolution defect localization and nanoscale electrical characterization.

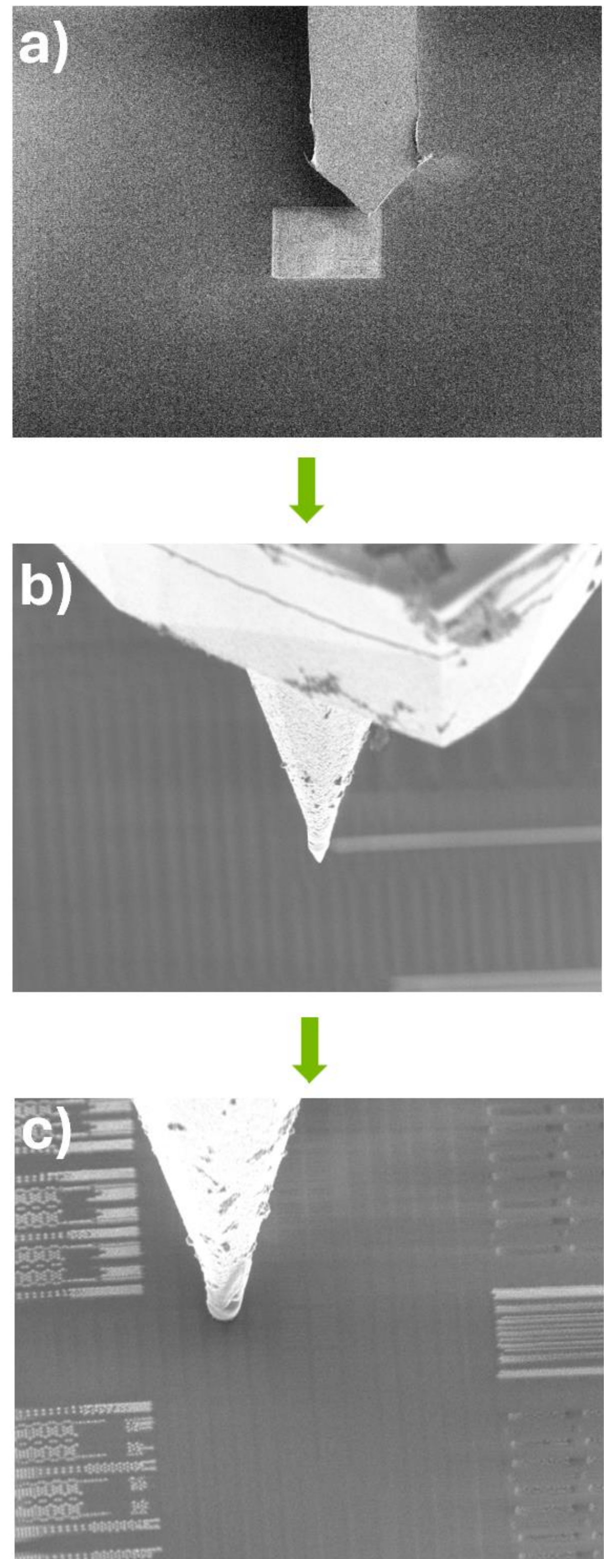

Figure 6. SEM images showing the process of guiding the AFM probe gradually to the exact target area for CAFM analysis a) AFM probe tip moved to the pFIB delayered window; b) AFM probe tip moved to the region of interest; c) AFM probe tip landed on the exact circuit of interest

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Once CAFM analysis at a given metallization or device layer is completed, the AFM probe tip can be safely retracted to its park position, and the system reconfigured into the milling mode (as illustrated in Figure 4) to enable further pFIB gas-assisted delayering to the next layer of interest. After delayering, the AFM probe is repositioned for scanning, and CAFM current imaging is performed again at the same area of interest, now at a lower level. This back-and-forth sequence between pFIB delayering and CAFM analysis can be repeated iteratively to get a thorough understanding of a layer-by-layer electrical characteristics of the target device or region.

Figure 7 presents CAFM current images acquired from 5nm logic cells at three different circuit levels, demonstrating the efficacy of this sequential delayering and analysis process. Similarly, Figure 8 shows current maps of 5nm static random-access memory (SRAM) bit-cells obtained at three distinct metallization levels, further confirming the reproducibility and precision of this approach across different device structures.

A key advantage of this integrated methodology is that the entire workflow, from delayering to imaging, is conducted within a single vacuum environment. This eliminates the need to break vacuum, transfer the sample between different instruments, or perform time-consuming re-navigation to the AOI after each analysis step. Conventional workflows typically require multiple tool transfers, each of which introduces the risk of surface oxidation, contamination, and potential misalignment. In contrast, the integrated system allows seamless mode switching with just a few user interactions, such as mouse clicks to reconfigure between milling and scanning modes, while maintaining pristine sample conditions and consistent probe alignment.

This streamlined process not only minimizes analysis time but also ensures high-quality, repeatable electrical measurements by preserving clean, oxide-free surfaces and precise spatial registration across successive layers. As a result, the integrated pFIB-AFM platform offers a powerful and efficient solution for high-resolution, multi-layer electrical characterization of advanced integrated circuits.

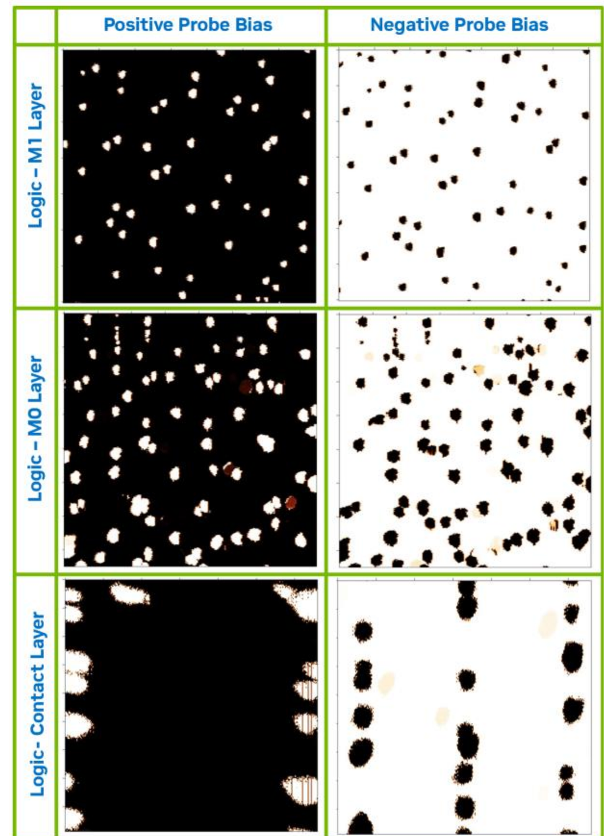

Figure 7. CAFM current images of logic cells after pFIB gas assisted delayering to three different layers

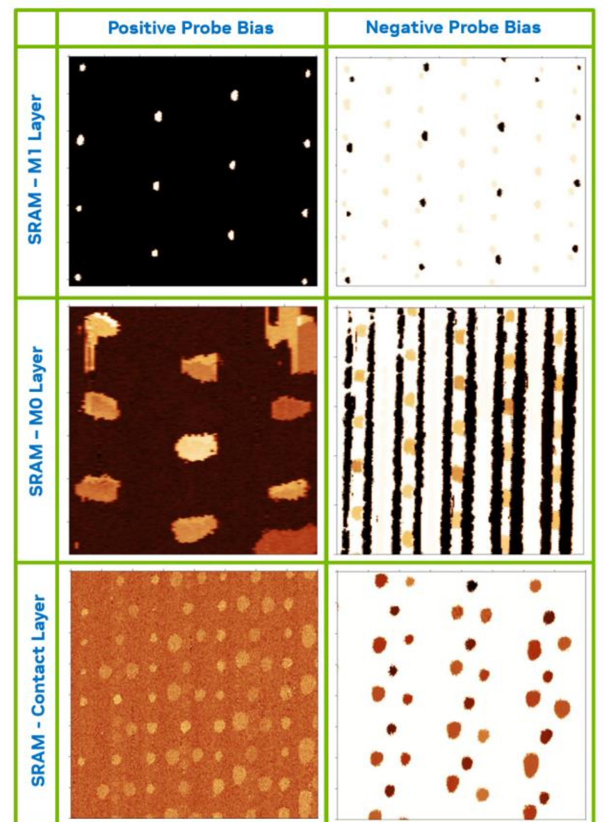

Figure 8. CAFM current images of SRAM bit-cells after pFIB gas assisted delayering to three different layers

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Beyond streamlining the entire CAFM sample preparation and analysis workflow, the integration of CAFM with electron beam (e-beam) capabilities within a pFIB/SEM system enables the development of novel imaging modalities. Specifically, the simultaneous movement of the e-beam and the AFM probe relative to the sample opens new possibilities for collecting and mapping characteristic electrical signals arising from the interaction of the electron beam with semiconductor devices. This synergy facilitates innovative applications that go beyond conventional CAFM use cases.

When a device is delayered to the contact level and exposed to an optimally configured electron beam, defined by parameters such as accelerating voltage, beam current, and E beam-to-AFM probe positioning, electron-beam-induced current (EBIC) can be generated and mapped. In this configuration, the CAFM probe collects EBIC current generated at each scanned point due to e-beam excitation of the underlying device structures. These currents often originate from electron-hole pair generation and subsequent carrier separation at p-n junctions within the semiconductor. The resulting EBIC signal reflects various junction properties.

This EBIC signal, captured in real time by the CAFM probe during raster scanning, can be reconstructed into a two-dimensional image that maps the junction behavior across the scanned area. We refer to this novel technique as Scanning EBIC Microscopy (SEBICM). It enables spatially resolved visualization of junction characteristics at the nanoscale, directly beneath individual contacts, a capability not easily accessible through traditional failure analysis methods.

Figure 9 illustrates the Scanning EBIC Microscopy concept and a representative result. In Figure 9a, a schematic cross-section shows the experimental setup: the electron beam interacts with a p+/N-well junction beneath the contact of a PFET device. The generated minority carriers recombine or are collected, producing a measurable EBIC signal, which is simultaneously captured by the conductive AFM probe scanning the contact surface. As both the e-beam and the AFM probe scan in synchrony across the device, the probe records variations in EBIC signal intensity that correspond to underlying junction characteristics.

Figure 9b presents a current image acquired using Scanning EBIC Microscopy from a logic cell region. Distinct current levels are observed at different contacts, reflecting variations in subsurface junction behavior. This technique has the potential for localized analysis of junction quality, enabling the detection of subtle junction-related anomalies, such as implantation defects, junction leakage, or doping non-uniformities, which may not be visible using conventional SEM PVC, or even stand-alone CAFM.

By revealing junction-level electrical contrast with high spatial resolution maps, Scanning EBIC Microscopy introduces a powerful new dimension to the failure analysis of advanced semiconductor devices.

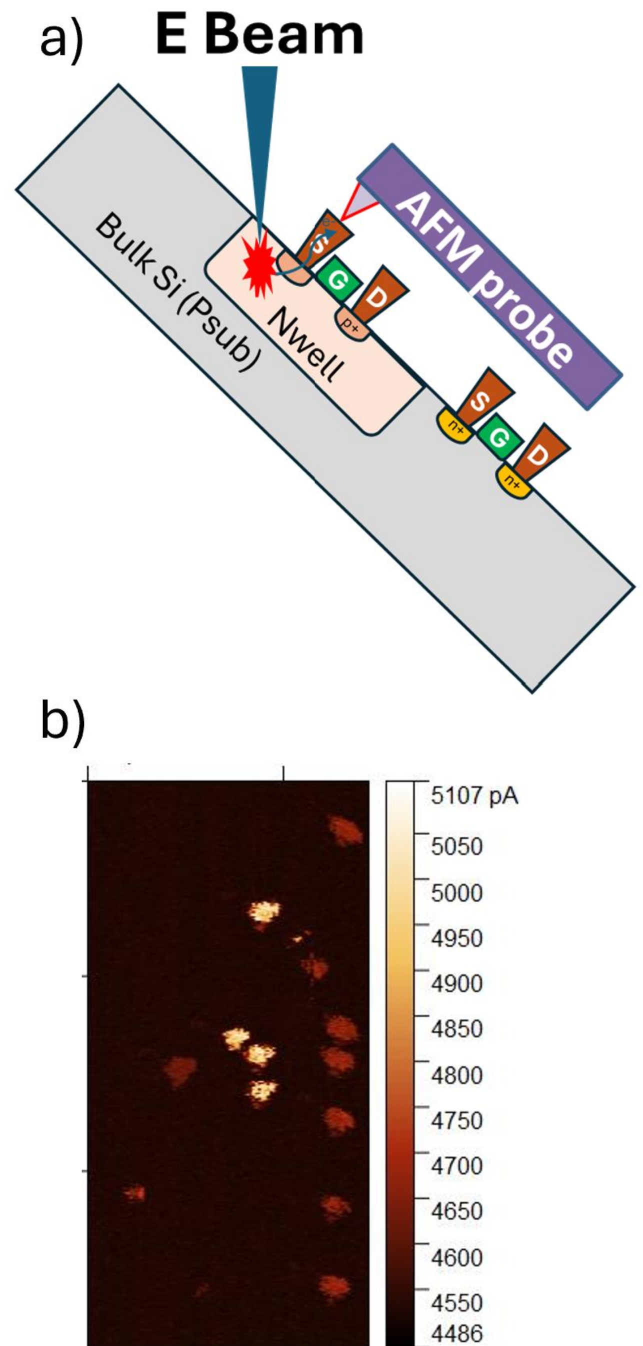

Figure 9. a) Schematics of scanning E-beam induced current microscopy; b) Current image collected with scanning E-beam induced current microscopy

Case Study: In-Situ Failure Analysis of a Stacked-Die Package

A chip with advanced heterogeneous package containing stacked IC die failed after an electrostatic discharge (ESD) test. The root cause was investigated using a direct physical failure analysis approach with an AFM in pFIB setup. A preliminary layout analysis identified a suspect circuit in one die within the

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die-stack, composed of hundreds of transistors connected in parallel by copper metallization layers.

The investigation began by mechanically lapping the package substrate to expose the suspect die. The top, thick metallization layers were further lapped off to reduce the time for subsequent pFIB delayering. The sample was then loaded into a compact AFM integrated within the pFIB chamber. Gas-assisted pFIB parallel milling, with real-time monitoring via SEM imaging, continued the delayering until the top level of the suspect circuit was exposed (Figure 10a). A CAFM current scan was immediately performed on the suspect circuit. While the AFM topography image (Figure 10b) showed well-resolved, uniform delayered structures, the initial CAFM current imaging failed to detect any abnormalities, as the current was extremely low across the entire area (Figure 10c).

This low current was attributed to a second die bonded beneath the failed die, which blocked the necessary current path. The standard CAFM technique requires a good electrical ground for the bulk silicon, allowing current to flow from the probe tip, through the device's p-n junctions, to the grounded AFM stage. The insulating die bonding material between the stacked dies prevented this, rendering the initial CAFM imaging ineffective as illustrated in Figure 10d. To solve this, a deep trench was milled near the suspect transistors (Figure 11a), extending into the die underneath to provide a ground path for the transistors' Nwell structure. This was performed precisely within the same pFIB chamber, eliminating the need to move the sample. In the subsequent CAFM current imaging, two structures that did not stand out in the previous CAFM image before creating the FIB grounding trench showed abnormally high current this time compared to neighboring reference structures (Figure 11b). A subsequent layout study revealed that the structures with elevated current were connected to a parallel array of transistor gates, indicating a defect in at least one of these gates. A schematic in Figure 11c illustrates how the pFIB-created trench allowed current to pass through the insulating die bonding material, enabling current imaging of this complex structure.

This integrated approach offered another unique advantage beyond the seamless switching between pFIB delayering and AFM analysis. The integration of an AFM within the pFIB enabled rapid, precise positioning of the AFM probe tip to the AOI, a crucial capability when working with delicate samples. In this specific case, the AOI was immediately adjacent to a deep trench created by the FIB. Traditional AFM analysis would have risked damaging the probe tip by scanning across this trench. However, using live SEM imaging, the AFM probe was precisely and efficiently positioned on the target area right next to the trench (Figure 11a) before the AFM scan began. This technique prevented the AFM probe's conductive tip from being damaged or worn out by unnecessarily scanning across the deep trench, and ensured a successful analysis.

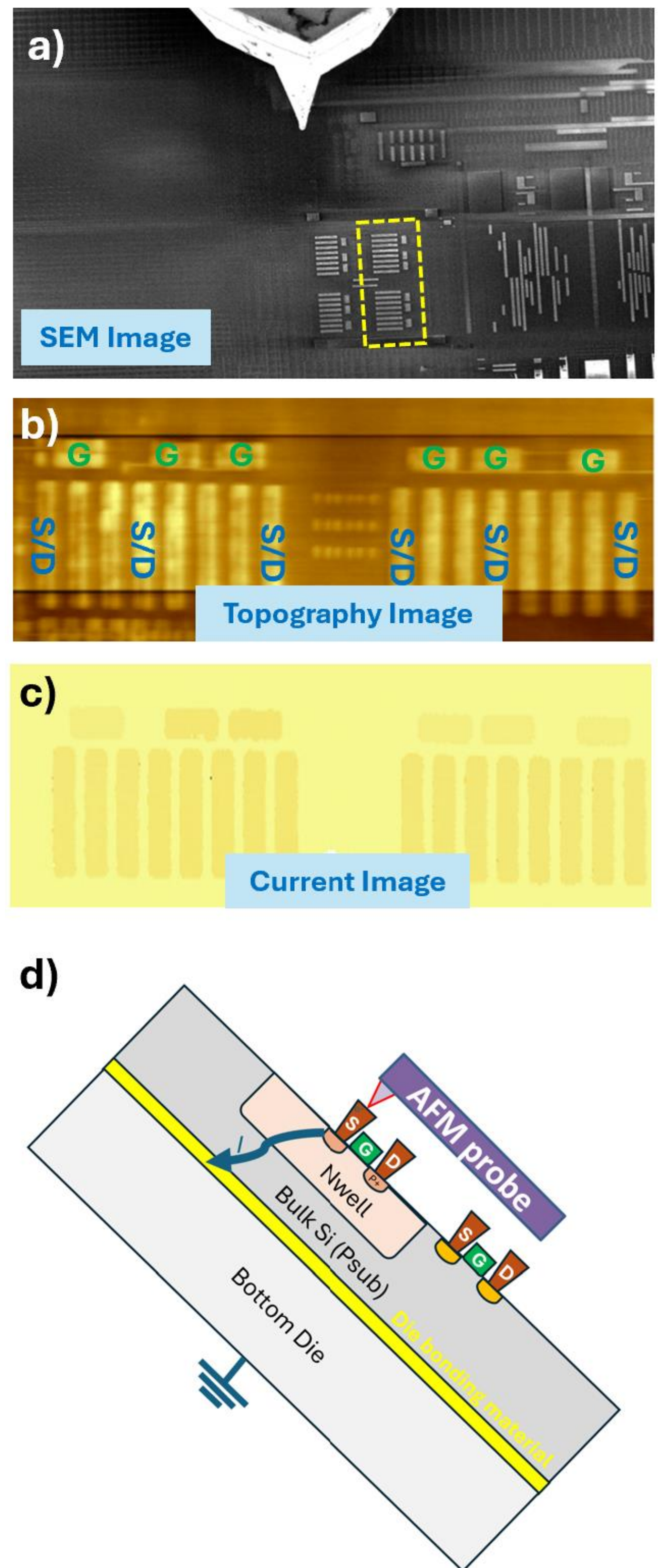

Figure 10. a) SEM image of the suspect circuit's top level, exposed by pFIB gas-assisted milling. b) AFM topography image of the exposed suspect circuit. (c) Initial CAFM current image of the suspect circuit, showing no abnormal current. d) Schematic illustrating how the die bonding material between the stacked dies blocks the current path required for CAFM imaging.

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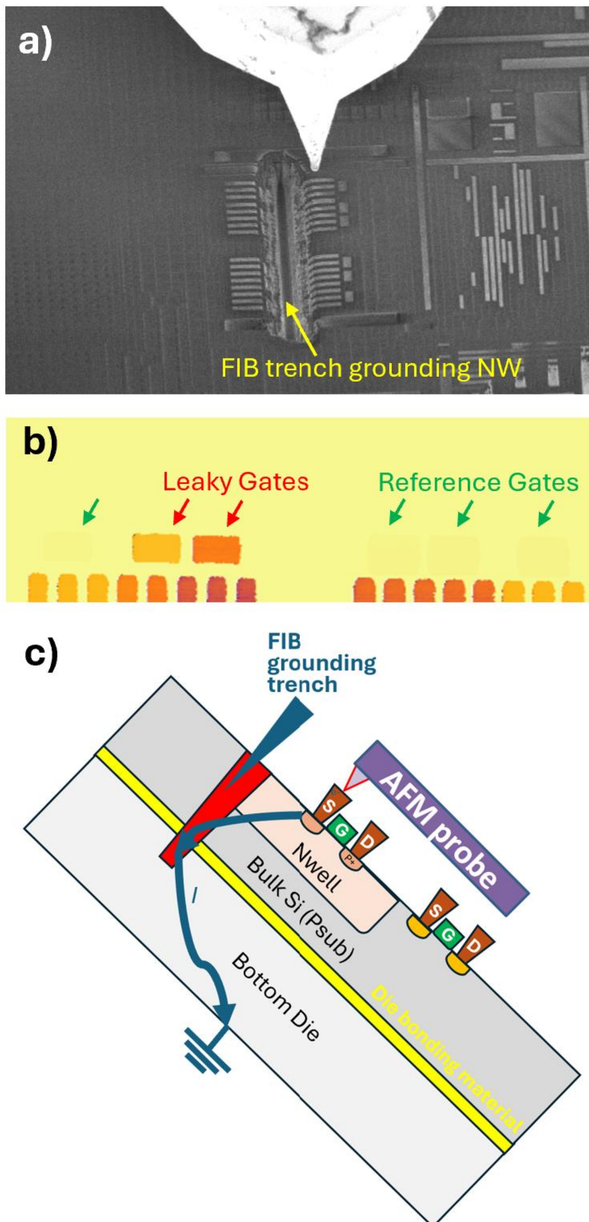

Figure 11. a) SEM image of the suspect circuit after using p-FIB to mill a deep trench for grounding the transistor well structure. b) CAFM current image of the suspect circuit, showing two structures with abnormally high current after the grounding trench was created. c) Schematic illustrating how the p-FIB-created trench allows current to pass through the insulating die bonding material, enabling successful CAFM analysis.

To further localize the defective gate, the die was then deprocessed using pFIB gas-assisted parallel milling to a lower level where the individual gates were separated. At this lower level, a second CAFM current imaging scan of the area containing this parallel array of transistor gates successfully identified two leaky gates with the abnormally high current (Figure 12). With the exact defect location identified, a leaky gate was able to be lifted out and thinned into a TEM lamella using FIB. Physical analysis of the leaky gate using transmission electron microscopy (TEM) found that the leakage was due to gate oxide breakdown, which was the ultimate cause of the chip failure.

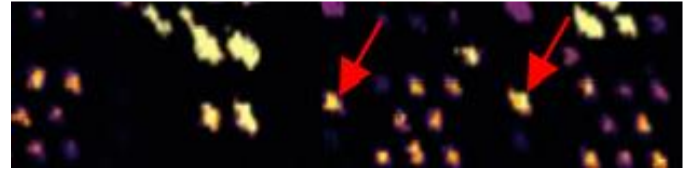

Figure 12. CAFM current image of the transistor level of the suspect circuit after pFIB milling to create a deep trench to ground the well structure of the suspect circuit

Conclusions

This work demonstrates the successful integration of a compact CAFM system into a pFIB/SEM dual-beam platform, creating a streamlined and efficient workflow for advanced IC failure analysis. By combining pFIB gas-assisted milling with in-situ CAFM current imaging, we eliminated the need for repeated vacuum cycles and manual sample transfers, which significantly reduced analysis time. This process also maintained pristine sample surface conditions, essential for high-quality CAFM current imaging. Furthermore, SEM-based navigation enhanced efficiency by enabling rapid and accurate positioning of the CAFM probe.

Through case studies involving logic and SRAM structures, we validated the ability to sequentially perform pFIB delayering and CAFM analysis on multiple layers with improved efficiency. We also introduced Scanning EBIC Microscopy, a novel imaging technique that provides spatially resolved maps of subsurface junction behavior, opening new possibilities for defect localization at the junction level. In one case study on a stacked-die package, the integrated system proved its effectiveness, with pFIB milling even being used to alter the circuit that enabled successful CAFM isolation.

Ultimately, this integration of CAFM with pFIB/SEM shows great promise for advancing semiconductor failure analysis, providing a powerful solution for localizing and characterizing defects in complex semiconductor devices.

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